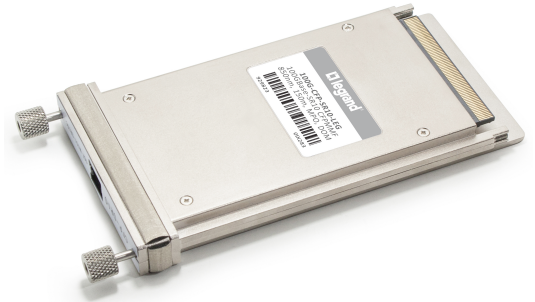


100G-CFP-SR10-LEG
BROCADE 100G-CFP2-LR4
850NM 150M REACH MPO DOM



Features

- Compliant to the CFP MSA Management Interface Specification Version 2.2
- Compliant to the CFP Hardware Specification Version 1.4
- Compliant to the IEEE 802.3ba(100GBASE-SR10)
- Transmission data rate up to 11.18 Gbit/s per channel
- Up to 300m on OM3 and 400m on OM4 MMF
- Power class 1 (<7W max)
- OTU4 compatible
- 10 channels 850nm VCSEL array transmitter
- 10 channels PIN photo detector array receiver
- MDIO digital diagnostic interface and control capabilities.
- TX input and RX output CDR retiming
- Hot pluggable electrical interface
- Operating case temperature: 0°C ~ +70°C
- Single 3.3V power supply
- RoHS 6 compliant(lead free)
- Utilizes a standard 24/20 lane optical fiber with MPO connector

Applications

- 100GBE interconnects
- High-speed core router connections & Datacom/Telecom switch
- Data aggregation and backplane applications
- Proprietary protocol and density application

Product Description

Legrand’s 100G-CFP-SR10-LEG Form Factor Pluggable CFP2 transceivers are compatible with the Small Form Factor Pluggable Multi-Sourcing Agreement (MSA). The CFP2 transceivers are high performance, cost effective modules supporting 100 Gigabit Ethernet and up to 150km transmission distance with SMF.

Legrand’s CFP transceivers are RoHS compliant and lead-free.

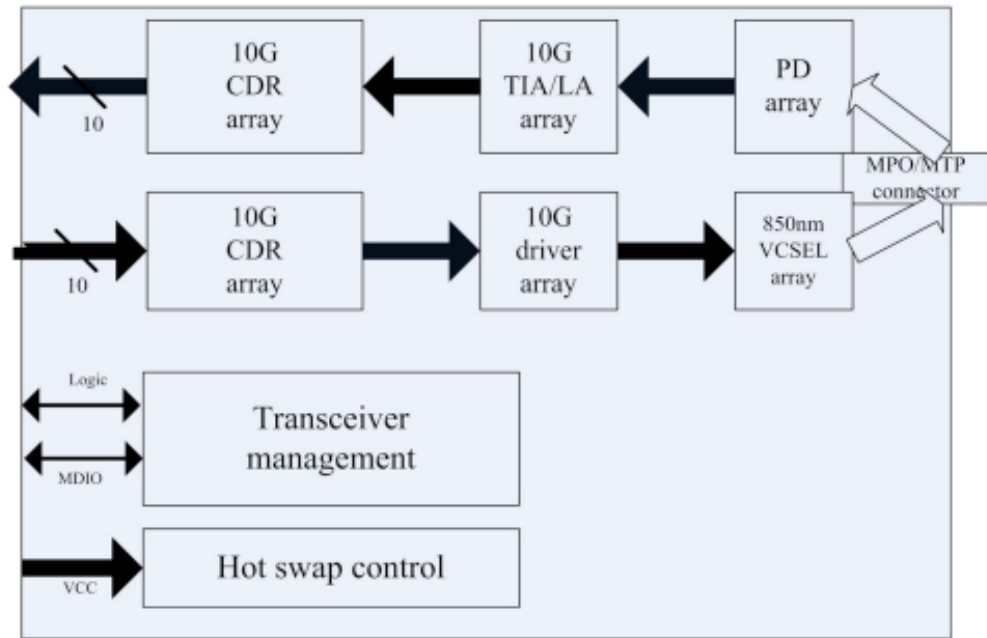


Figure 1. Module Bock Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{cc}	-0.5	3.6	V
Input Voltage	V_{in}	-0.3	$V_{cc}+0.3$	V
Storage Temperature	T_{st}	-40	85	°C
Humidity (non-condensing)	R_h	5	85	%

*Exceeding any one of these values may destroy the device immediately

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Operating Case Temperature	T_{ca}	0		70	°C

Data Rate Per Lane	Fd	-	10.3125	11.18	Gbps
Power Dissipation	Pm			7	W
Lower Power Mode Dissipation	P _{low}			2	W
Aggregate Bit Rate	BR _{aggr}		103.125	111.8	Gbps

Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Differential Input Impedance	Z _{in}	90	100	110	ohm	
Differential Output Impedance	Z _{out}	90	100	110	Ohm	
Differenetial Input Voltage and Amplitude	△V _{in}	120		820	mVp-p	
Differential Output Voltage Amplitude	△V _{out}	300		820	mVp-p	
Input Logic Level High	V _{IH}	2.0		VCC+0.3	V	3.3V LVCOMS
		0.84		12	V	1.2V LVCOMS
Input Logic Level Low	V _{IL}	-0.3		0.8	V	3.3V LVCOMS
		-0.3		0.36	V	1.2V LVCOMS
Output Logic Level High	V _{OH}	VCC-0.2		VCC	V	3.3V LVCOMS
		1.0		1.5	V	1.2V LVCOMS
Output Logic Level Low	V _{OL}	0		0.2	V	3.3V LVCOMS
		-0.3		0.2	V	1.2V LVCOMS

Note:

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measuered between RxnP and RxnN.

Optical Characteristics

Transmitter Optical Specifications (T= 25°C, VCC= 3.3V +/- 5%)

Parameter	Symbol	Min.	Typical	Max.	Unit
Average Optical Power (per channel)	P _{out}	-7.6	-1	+2.4	dBm
Average Optical Power (per channel) – Disabled	P _{off}			-30	dBm
Optical Return Loss Tolerance				12	dB
Extinction Ratio	ER	3			dB
Center Wavelength	λ _C	840	850	860	Nm
RMS Spectral Width	λ		0.5	0.65	Nm
Transmit OMA per Lane	TX_OMA/lane	-5.6		3	dBm
Difference in launch power between any two lanes (OMA)				4	dB

Transmitter and dispersion penalty each lane	TDP/lane			3.5	dB
Transmitter eye mask	Compliant to IEEE802.3ba eye mask specification				

Note:

1. Average optical power is measured at the output of the modules optical interface.

Receiver Optical Specifications (T= 25°C, VCC= 3.3V +/- 5%)

Parameter	Symbol	Min.	Typical	Max.	Unit
Optical Power Sensitivity (per channel)	Pin min	-	-12	-9.9	dBm
Optical Power Saturation (per channel)	Pin max	+1	-	-	dBm
Stressed Receiver Sensitivity	P _s	-	-	-5.4	dBm
Center Wavelength	λ _C	840	850	860	Nm
RMS Spectral Width	λ		0.5	0.65	Nm
Optical Return Loss	RI	12			dB
Damage Threshold		3.4			dBm
Optical Modulation Amplitude Each Lane				3	dBm

Note:

1. Optical power sensitivity is measured with BER@10⁻¹² at 10.3125Gbps per channel.

CFP Module Functional Block Diagram

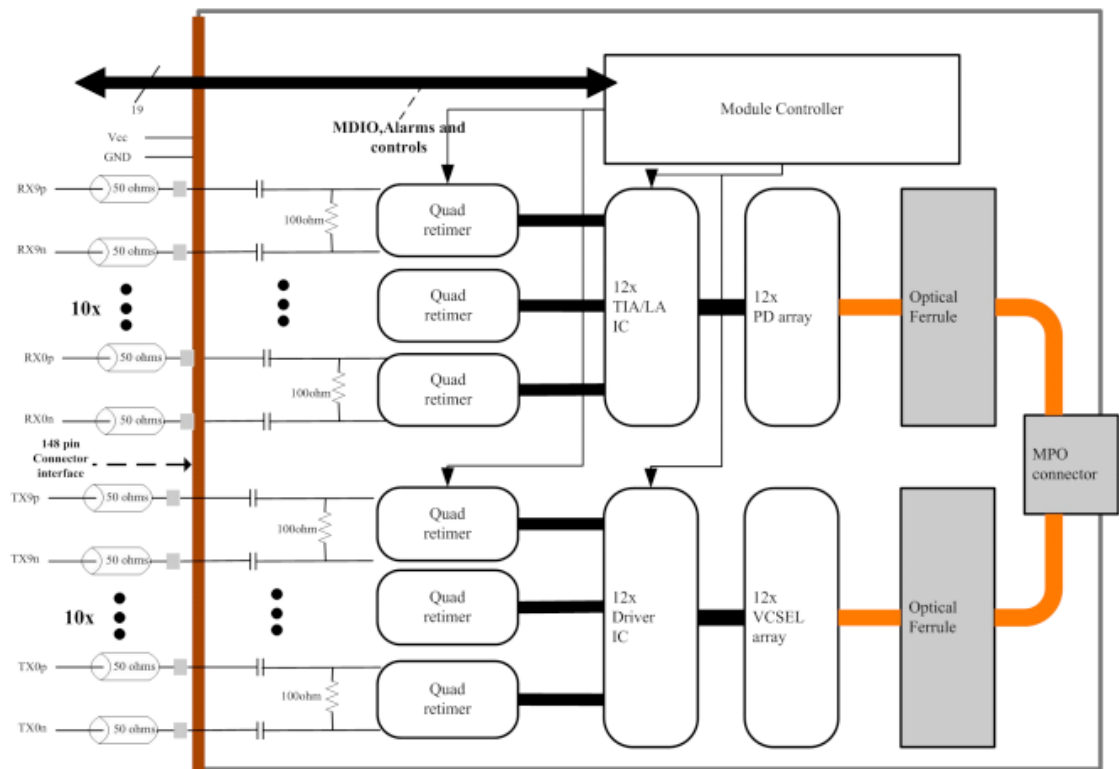


Figure 2. CFP Module Functional Block Diagram

Pin Descriptions

Part A: Bottom Row Pin Function Definition

Pin	Symbol	Type	I/O	Description
1	3.3V_GND	GND		3.3V Module Supply Voltage Return Ground, can be separate or tied together with signal ground
2	3.3V_GND	GND		
3	3.3V_GND	GND		
4	3.3V_GND	840 GND		
5	3.3V_GND	GND		
6	3.3V	VCC		3.3V Module Supply
7	3.3V	VCC		
8	3.3V	VCC		
9	3.3V	VCC		
10	3.3V	VCC		

11	3.3V	VCC		
12	3.3V	VCC		
13	3.3V	VCC		
14	3.3V	VCC		
15	3.3V	VCC		
16	3.3V_GND	GND		
17	3.3V_GND	GND		
18	3.3V_GND	GND		
19	3.3V_GND	GND		
20	3.3V_GND	GND		
21	NC		I/O	Gigalight internal, do not connect
22	NC		I/O	Gigalight internal, do not connect
23	GND	GND		
24	(TX_MCLKn)	CML	O	CML For optical waveform testing. Not used.
25	(TX_MCLKp)	CML	O	CML For optical waveform testing. Not used.
26	GND	GND		
27	NC		I/O	Gigalight internal, do not connect
28	NC		I/O	Gigalight internal, do not connect
29	NC		I/O	Gigalight internal, do not connect
30	PRG_CNTL1	LVC MOSw/PU	I	Programmable Control 1 set via MDIO, MSA default: TRXIC_RSTn – TX & RX IC reset. “0” – reset, “1” or NC = enabled or not used
31	PRG_CNTL2			Programmable Control 2 set via MDIO, MSA default: Hardware power Interlock LSB, “00” = <8W, “01” = <16W, “10” < 24W, “11” or NC = > 24W or not used
32	PRG_CNTL3			Programmable Control 3 set via MDIO, MSA default: Hardware power Interlock MSB, “00” = <8W< “01” = <16W, “10” < 24W, “11” or NC = > 24W or not used
33	PRG_ALARM1	LVC MOS	O	Programmable Alarm 1 set via MDIO, Reflex default: HIPWR_ON, Module power on indicator. “1” = Module high power up completed, “0” = Module not high powered up
34	PRG_ALARM2	LVC MOS	O	Programmable Alarm 2 set via MDIO, Reflex default: MOD_READY, module initialization complete, “1” = complete, “0” = not complete

35	PRG_ALARM3	LVC MOS	O	Programmable Alarm 3 set via MDIO, Reflex default: MOD_FAULT, module fault detected, “1” fault, “0” = no fault
36	TX_DIS	LVC MOSw/PU	I	Transmitter Disable for all channels, “1” or NC = transmitter disabled, “0” = transmitter enabled
37	MOD_LOPWR	LVC MOSw/PU	I	Module low power mode. “1” or NC = module in low power (safe) mode, “0” = power-on enabled
38	MOD_ABS	GND	O	Module Absent. “1” or NC = Module absent, “0” = module present. Pull-up resistor on Host
39	MOD_RSTn1	LVC MOSw/PD	I	Module Reset. “0” = reset the module, “1” or NC = module enabled, Pull Down resistor in module
40	RX_LOS	LVC MOS	O	Receiver loss of optical signal on any channel, “1” = loss of signal, “0” = normal condition
41	GLB_ALRMn	LVC MOS	O	Global Alarm. “0” = alarm condition in any MDIO alarm register, “1” = no alarm
42	PRTADR4	1.2V CMOS	I	MDIO port address bit 4
43	PRTADR3	1.2V CMOS	I	MDIO port address bit 3
44	PRTADR2	1.2V CMOS	I	MDIO port address bit 2
45	PRTADR1	1.2V CMOS	I	MDIO port address bit 1
46	PRTADR0	1.2V CMOS	I	MDIO port address bit 0
47	MDIO	1.2V CMOS	I/O	Management Data I/O bi-directional data (electrical specs as per 802.3ae)
48	MDC	1.2V CMOS	I	Management data clock (electrical specs as per 802.3ae)
49	GND	GND		
50	NC			Gigalight internal, do not connect
51	NC			Gigalight internal, do not connect
52	GND	GND		
53	NC		I/O	Gigalight internal, do not connect
54	NC		I/O	Gigalight internal, do not connect
55	3.3V_GND	GND		3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
56	3.3V_GND	GND		
57	3.3V_GND	GND		
58	3.3V_GND	GND		
59	3.3V_GND	GND		

60	3.3V	VCC		3.3V Module Supply
61	3.3V	VCC		
62	3.3V	VCC		
63	3.3V	VCC		
64	3.3V	VCC		
65	3.3V	VCC		
66	3.3V	VCC		
67	3.3V	VCC		
68	3.3V	VCC		
69	3.3V	VCC		
70	3.3V_GND	GND		
71	3.3V_GND	GND		
72	3.3V_GND	GND		
73	3.3V_GND	GND		
74	3.3V_GND	GND		

Part B: Top Row Pin Function Definition

Pin	Symbol		Pin	Symbol
148	GND		111	GND
147	Not used		110	Not used
146	Not used		109	Not used
145	GND		108	GND
144	Not used		107	RX9n
143	Not used		106	RX9p
142	GND		105	GND
141	TX9n		104	RX8n
140	TX9p		103	RX8p
139	GND		102	GND
138	TX8n		101	RX7n
137	TX8p		100	RX7p
136	GND		99	GND
135	TX7n		98	RX6n

134	TX7p		97	RX6p
133	GND		96	GND
132	TX6n		95	RX5n
131	TX6p		94	RX5p
130	GND		93	GND
129	TX4n		92	RX4n
128	TX4p		91	RX4p
127	GND		90	GND
126	TX4n		89	RX3n
125	TX4p		88	RX3p
124	GND		87	GND
123	TX3n		86	RX2n
122	TX3p		85	RX2p
121	GND		84	GND
120	TX2n		83	RX1n
119	TX2p		82	RX1p
118	GND		81	GND
117	TX1n		80	RX0n
116	TX1p		79	RX0p
115	GND		78	GND
114	TX0n		77	Not used
113	TX0p		76	Not used
112	GND		75	GND

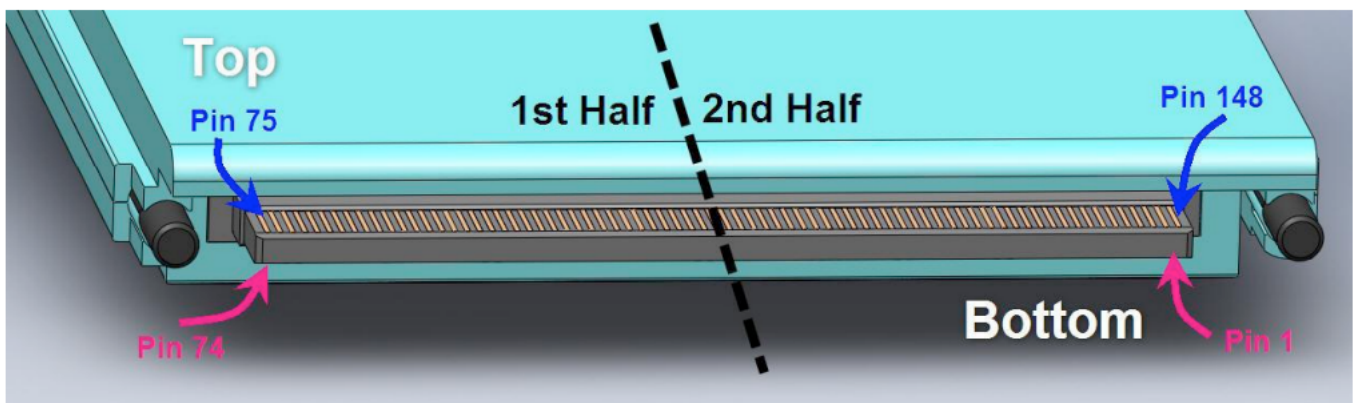


Figure 3. Pad Layout of the CFP Module

CFP Optical Interface Lanes and Assignment

Figure 3 shows the orientation of the multimode fiber facets of the optical connector

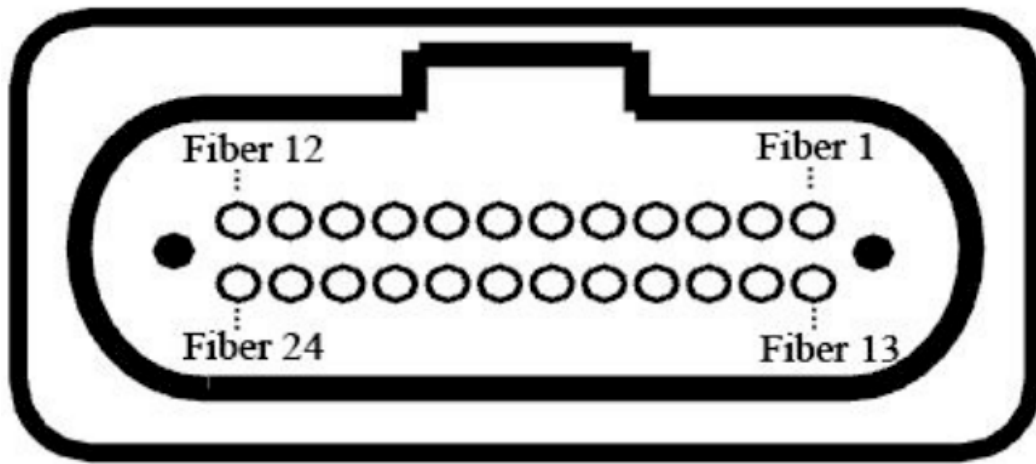


Figure 4. Outside view of the CFP Module MPO Receptacle

Lane Assignment

Fiber	Symbol	Corresponding Electrical Pins	Fiber	Symbol	Corresponding Electrical Pins
1	Unused		13	Unused	
2	RX0	79, 80	14	TX0	113, 114
3	RX1	82, 83	15	TX1	116, 117
4	RX2	85, 86	16	TX2	119, 120
5	RX3	88, 89	17	TX3	122, 123
6	RX4	91, 92	18	TX4	125, 126
7	RX5	94, 95	19	TX5	128, 129
8	RX6	97, 98	20	TX6	131, 132
9	RX7		21	TX7	134, 135
10	RX8		22	TX8	137, 138
11	RX9		23	TX9	140, 141
12	Unused		24	Unused	

Mechanical Dimensions

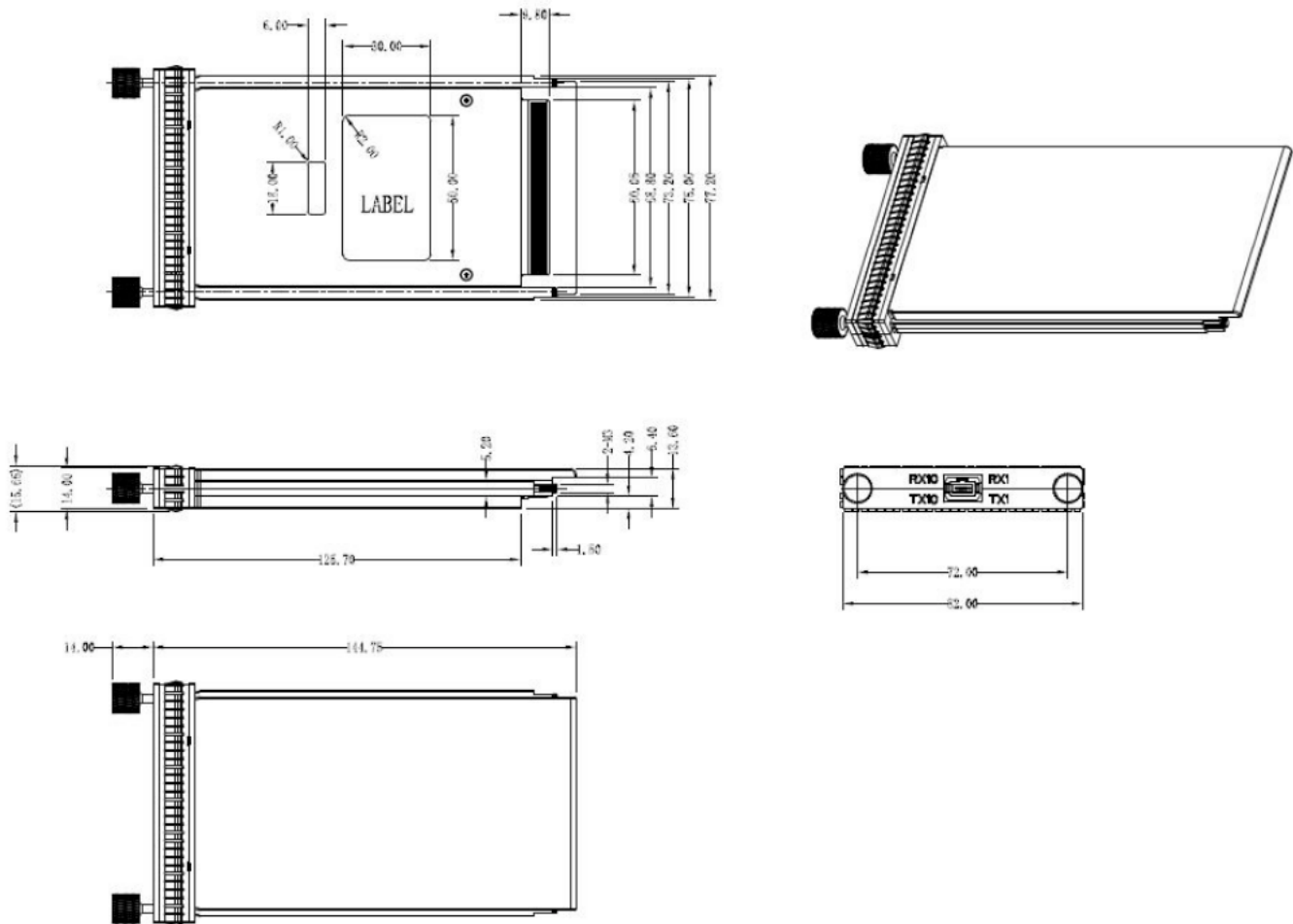


Figure 5. Mechanical Specifications



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