QSFP-H40G-LEGC3M-LEG
CISCO 40GBASE-AOC QSFP+
850NM 3M ACTIVE OPTICAL

QSFP-H40G-LEGC3M-LEG
40Gbase QSFP+ Cable

Features

- Full duplex 4 channel 850nm parallel active optical cable
- Transmission data rate up to 10.3Gbit/s per channel
- SFF-8436 QSFP+ compliant
- Hot pluggable electrical interface
- Differential AC-coupled high speed data interface
- 4 channels 850nm VCSEL array
- 4 channels PIN photo detector array
- Low power consumption <1.5W
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 6 compliant

Applications

- Infiniband transmission at 4ch SDR, DDR and QDR
- 40GBASE-SR4 Ethernet
- Data Centers

Product Description

Legrand's QSFP-H40G-LEGC3M-LEGQSFP active optic cables are a high performance, low power consumption, long reach interconnect solution supporting 40G Ethernet, fiber channel and PCIe. It is compliant with the QSFP MSA and IEEE P802.3ba 40GBASE-SR4. QSFP AOC is an assembly of 4 full-duplex lanes, where each lane is capable of transmitting data at rates up to 10Gb/s, providing an aggregated rate of 40Gb/s.

Legrand's QSFP+ transceivers are RoHS compliant and lead-free.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	-0.5		4.0	V
Input Voltage	Vin	-0.3		Vcc+0.3	V
Storage Temperature	Ts	-20		85	°C
Case Operating Temperature	Top	0		70	°C
Humidity (non-condensing)	RH	5		95	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case Temperature	Tca	-5		70	°C
Data Rate Per Lane	fd	2.5		10.3	Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm			1.5	W
Fiber Band Radius	Rb	3			cm

Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential input impedance	Zin	90	100	110	ohm	2
Differential Output impedance	Zout	90	100	110	ohm	3
Differential input voltage amplitude	ΔVin	300		1100	mVp-p	
Differential output voltage amplitude	ΔVout	500		800	mVp-p	
Skew	Sw			300	ps	
Bit Error Rate	BR			E-12		
Input Logic Level High	VIH	2.0		Vcc	V	
Input Logic Level Low	VIL	0		0.8	V	
Output Logic Level High	VOH	Vcc-0.5		Vcc	V	
Output Logic Level Low	VOL	0		0.4	V	

Notes:

1. BER=10^-12; PRBS 2^31-1@10.3125Gbps.
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxNP and RxnN.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Center Wavelength	λC	840	850	860	nm	
RMS Spectral Width	Δλ			0.65	nm	
Average Launch Power per Channel	Pout	-7.5		-2.5	dBm	
Difference in launch power between any two lanes (OMA)					dB	

Extinction Ratio	ER	3			dB	
Peak power, each lane				4	dBm	
Transmitter and dispersion penalty (TDP), each lane	TDP			3.5	dB	
Average launch power of OFF transmitter, each lane				-30	dB	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		0.23, 0.34, 0.43, 0.27, 0.33, 0.4				Hit Ratio = 5x10-5
Receiver						
Center Wavelength	λC	840	850	860	nm	
Stressed receiver sensitivity in OMA, each lane				-5.4		1
Maximum Average power at receiver input, each lane				2.4		
Receiver Reflectance				-12		
Peak power, each lane				4		
LOS Assert		-30				
LOS De-Assert – OMA				7.5		
LOS Hysteresis		0.5				

Note:

1. Measured with conformance test signal at TP3 for BER = 10e-12

Pin Descriptions

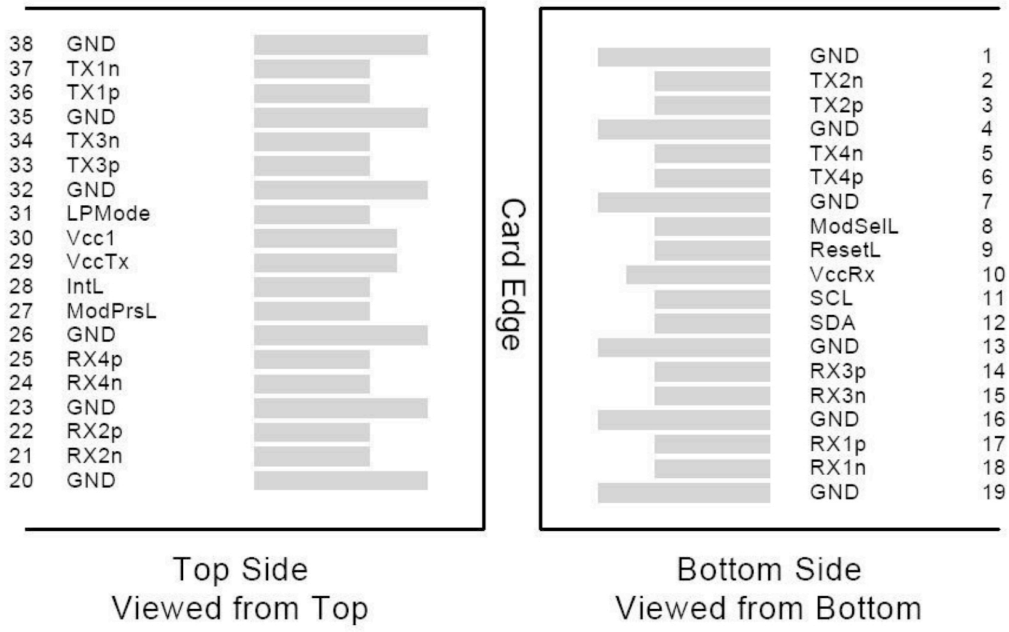
Pin	Logic	Symbol	Name/Descriptions	Ref.
1		GND	Module Ground	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module Ground	1
5	CML-I	Tx4-	Transmitter inverted data input	
6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module Ground	1
8	LVTTL-I	MODSEIL	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10		VCCRx	+3.3v Receiver Power Supply	
11	LVCMOS-I/O	SCL	2-wire Serial interface clock	2
12	LVCMOS-I/O	SDA	2-wire Serial interface data	2

13		GND	Module Ground	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted dta output	
16		GND	Module Ground	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module Ground	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	
26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board	2
29		VCCTx	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Module Ground	1
33	CML-I	Tx3+	Transmitter non-inverted data input	
34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	

Note:

1. GND is the symbol for signal and supply (power), Connect these directly to the host board signal common ground plane
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP+. The connector pins are each rated for a maximum current of 500mA.

Pin Assignment and Pin Description



ModSeIL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Operate in the low power mode (less than 1.5 W power consumption) This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

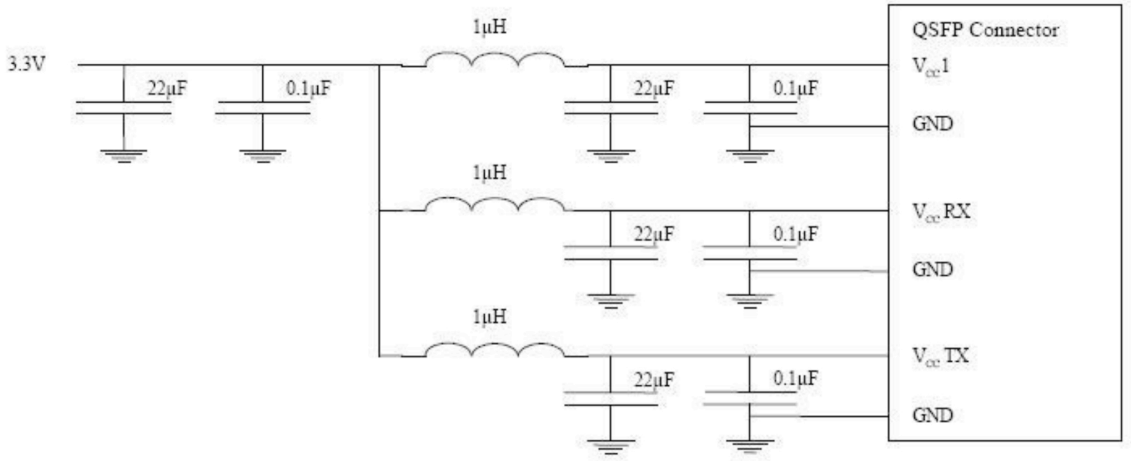
ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and de-asserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

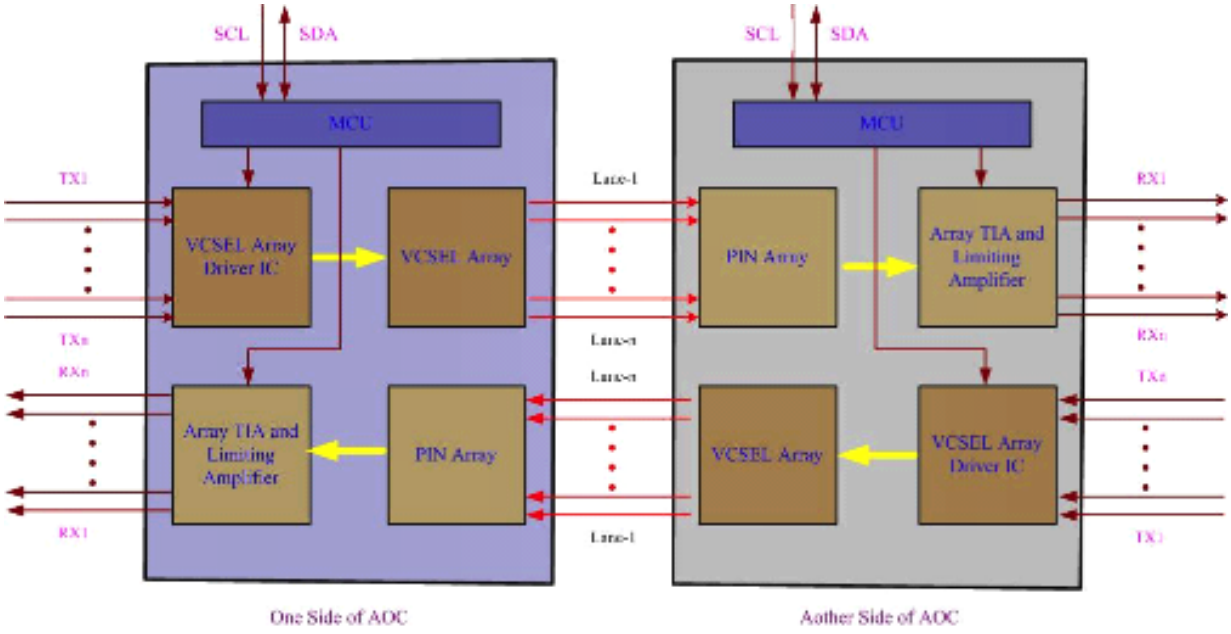
The host board should use the power supply filtering shown below.



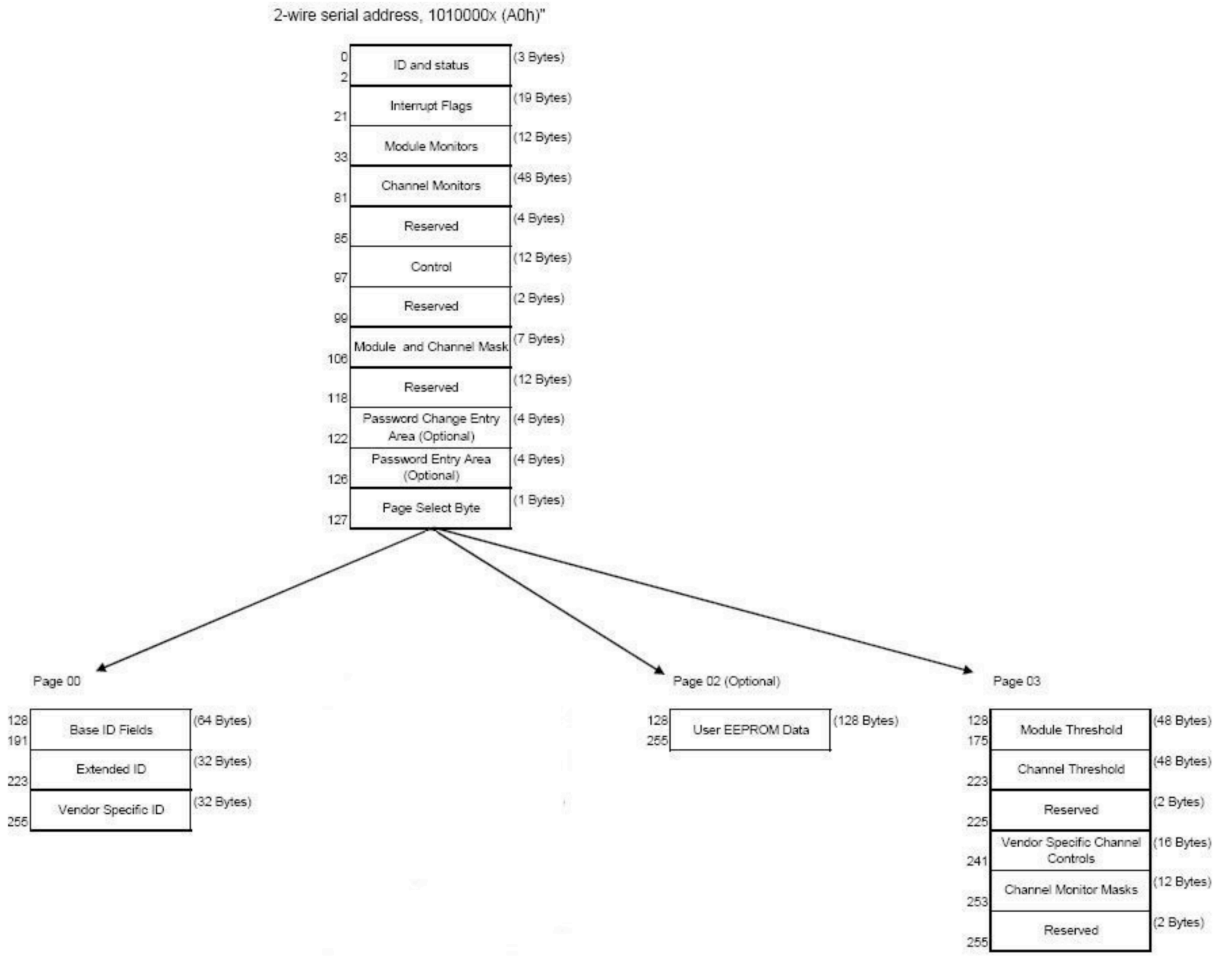
DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all QSFP AOCs. A 2-wire serial interface provides user to contact with module. The structure of the memory is shown in Figure 4. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

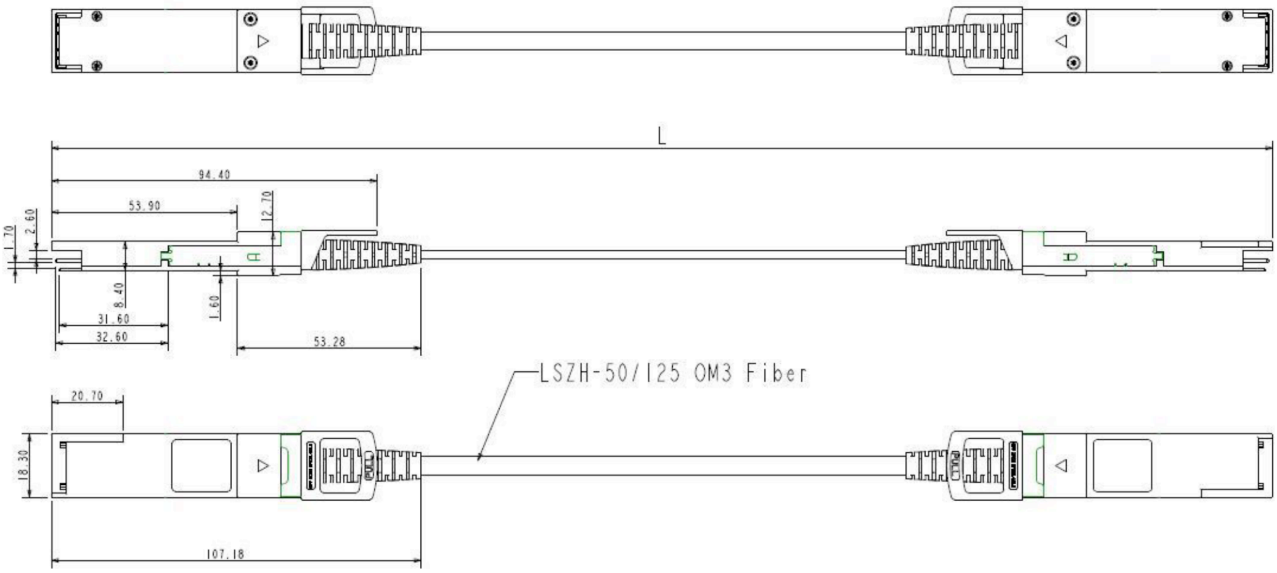
Module Block Diagram



Memory Map



Mechanical Specifications



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