WSP-Q40GLR4L-LEG
CISCO 40GBASE-LR4 QSFP+ SMF
1310NM 1.4M REACH MPO DOM PARALLEL

WSP-Q40GLR4L-LEG
40Gbase QSFP+ Transceiver

Features

- Four-Channel full-duplex transceiver modules
- Transmission data rate up to 11.2Gbit/s per channel
- Aggregate bandwidth of up to 44.0G
- QSFP+ MSA compliant
- Up to 1.4km transmission on single mode fiber (SMF)
- Maximum power consumption 3.5W
- Single +3.3V power supply
- Operating case temperature: 0 to 70°C
- RoHS-6 compliant
- TX: 1310nm FP
- RX: PIN

Applications

- InfiniBand FDR
- 16x Fibre Channel
- PCI-e3.0
- Proprietary High Speed Interconnections
- SAS 3.0

Product Description

Legrand's WSP-Q40GLR4L-LEG Quad Small Form Factor Pluggable (QSFP+) transceivers are compatible with the Small Form Factor Pluggable Multi-Sourcing Agreement (MSA). The QSFP+ transceivers are high performance, cost effective modules supporting 40 Gigabit Ethernet and up to 1.4m transmission distance with SMF.

Legrand's QSFP+ transceivers are RoHS compliant and lead-free.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	-0.3		3.6	V
Input Voltage	Vin	-0.3		Vcc+0.3	V
Storage Temperature	Tst	-20		85	°C
Case Operating Temperature	Top	0		70	°C
Humidity (non-condensing)	Rh	5		95	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case Temperature	Tca	0		70	°C
Data Rate Per Lane	fd	2.5		14.025	Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm			1.5	W
Fiber Bend Radius	Rb	3			cm

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Input impedance	Zin	90	100	110	ohm	
Differential Output impedance	Zout	90	100	110	ohm	
Differential Input Voltage amplitude	ΔVin	300		1100	mVp-p	
Differential output voltage amplitude	ΔVout	500		800	mVp-p	
Skew	Sw			300	ps	
Bit Error Rate	BR			E-12		
Input Logic Level High	VIH	2.0		VCC	V	
Input Logic Level Low	VIL	0		0.8	V	
Output Logic Level High	VOH	VCC-0.5		VCC	V	
Output Logic Level Low	VOL	0		0.4	V	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Center Wavelength	λC	1260	1310	1355	nm	
RMS Spectral Width	Δλ			3.5	nm	
Average Launch Power	P_T			7.5		
Average Optical Power per Channel	P_{AVG}	-5.5		1.5	dBm	
Optical Modulation Amplitude (OMA), each lane	P_{OMA}	-4.5		2.5	dBm	
Difference in launch power between any two lanes (OMA)				6.5	dB	

Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-5.5			dBm	
TDP, each Lane	TDP			3.2	dB	
Extinction Ratio	ER	3.5			dB	
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss Tolerance	TOL			12	dB	
Transmitter Reflectance	R_T			-12	dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Eye Mask Coordinates: X1, X2, X3, Y1, Y2, Y3	Specification Values {0.25, 0.4, 0.45, 0.25, 0.28, 0.4}					
Receiver						
Center Wavelength	λC	1260	1310	1355	nm	
Damage Threshold, each Lane	TH_d	3.3			dBm	
Average Receive Power, each Lane		-11.5		1.5	dBm	
Receiver Reflectance				-12	dB	
Peak power, each lane				2.5	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-11.5	dBm	
Difference in Receive Power between any Two Lanes (OMA)	Prx,diff			7.5	dB	
LOS Assert	LOSA	-30			dBm	
LOS Deassert	LOSD			-15	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane	Fe			12.3	GHz	

Note:

1. Measured with conformance test signal at TP3 for BER = 10e-12

Pin Descriptions

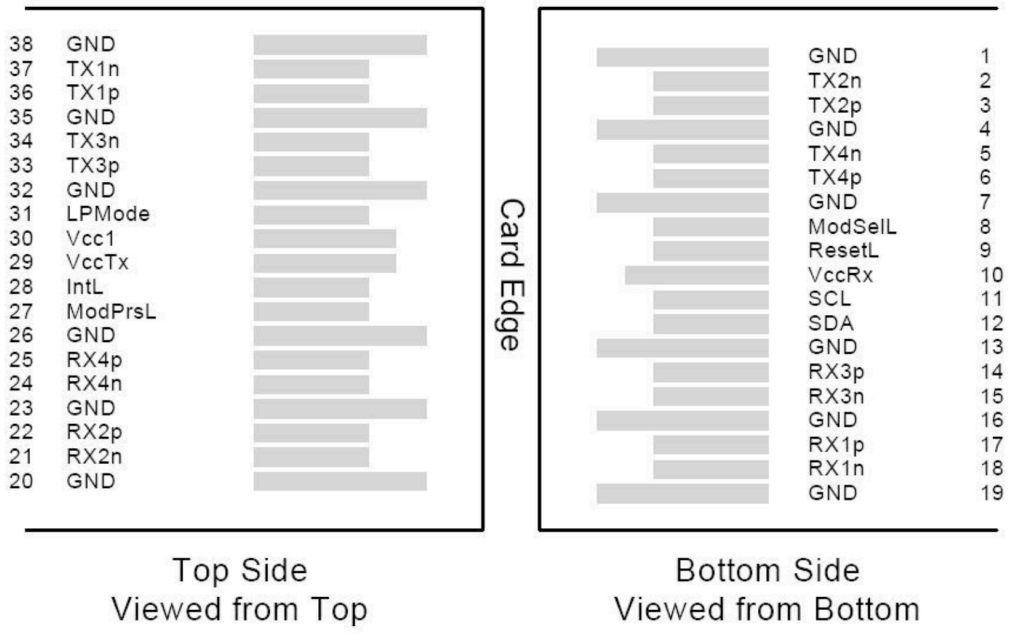
Pin	Logic	Symbol	Name/Descriptions	Ref.
1		GND	Module Ground	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module Ground	1
5	CML-I	Tx4-	Transmitter inverted data input	
6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module Ground	1
8	LVTTL-I	MODSEIL	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10		VCCRx	+3.3v Receiver Power Supply	
11	LVCMOS-I	SCL	2-wire Serial interface clock	2
12	LVCMOS-I/O	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted dta output	
16		GND	Module Ground	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module Ground	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	
26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board	2
29		VCCTx	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Module Ground	1
33	CML-I	Tx3+	Transmitter non-inverted data input	

34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	
38		GND	Module Ground	1

Note:

1. Module circuit ground is isolated from module chassis ground with in the module.
2. Open collector; should be pulled up with 4.7k-10k ohms on host board to a voltage between 3.15V and 3.6V.

Electrical Pin-out Details



ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the

ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Operate in the low power mode (less than 1.5 W power consumption) This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

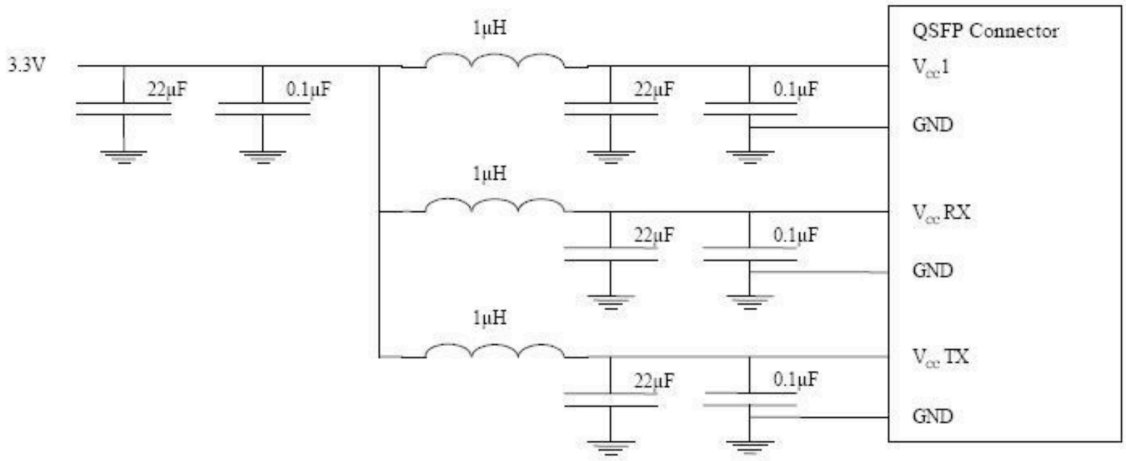
ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and de-asserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

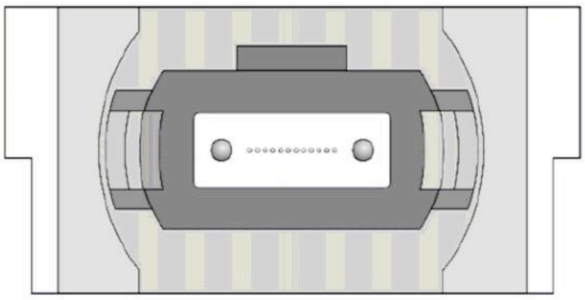
Power Supply Filtering

The host board should use the power supply filtering shown below.



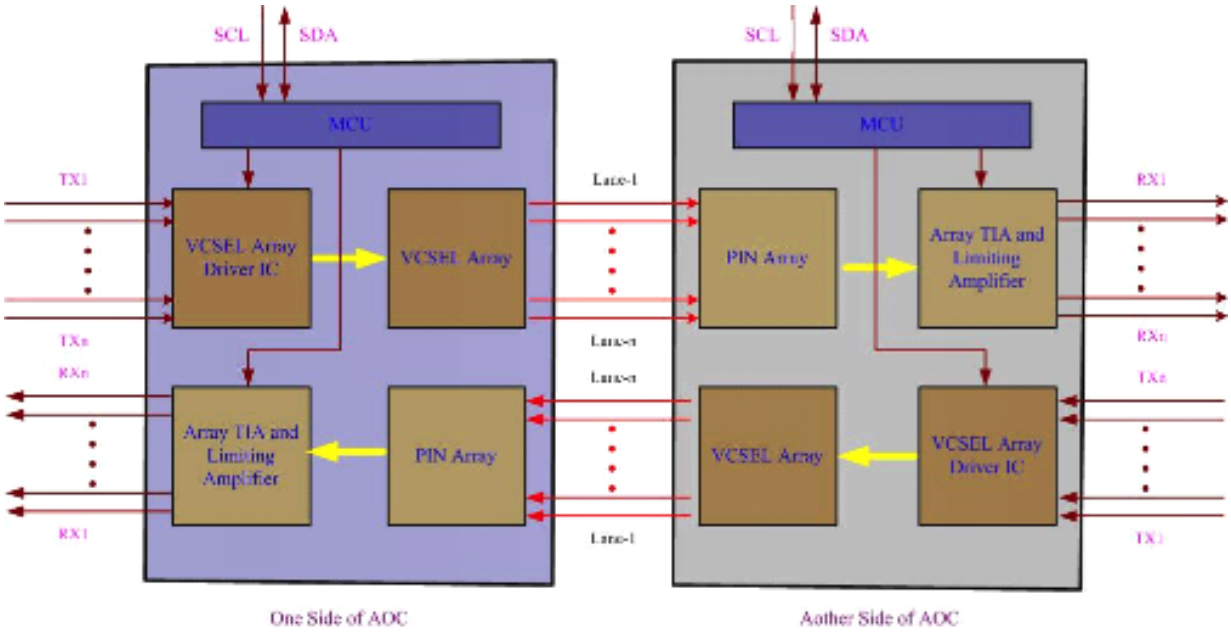
Optical Interface Lanes and Assignment

The optical interface port is a male MPO connector .The four fiber positions on the left as shown below, with the key up, are used for the optical transmit signals (Channel 1 through 4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1). The central four fibers are physically present.

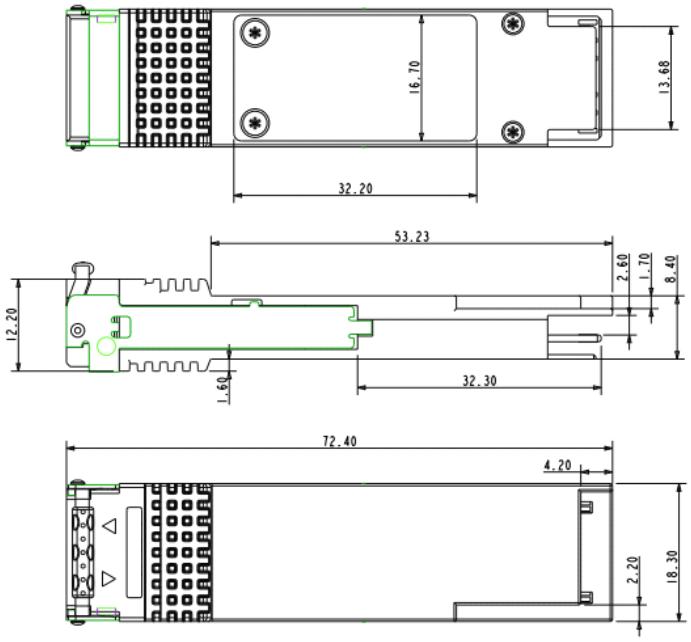


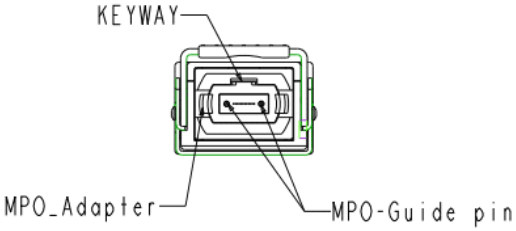
Transmit Channels: 1 2 3 4
Unused positions: x x x x
Receive Channels: 4 3 2 1

Module Block Diagram



Mechanical Specifications





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